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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/728,398

12/05/2003

William C. Moyer

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FREESCALE SEMICONDUCTOR, INC.  
LAW DEPARTMENT  
7700 WEST PARMER LANE MD:TX32/PL02  
AUSTIN, TX 78729

EXAMINER

MEHRMANESH, ELMIRA

ART UNIT

PAPER NUMBER

2113

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/728,398	MOYER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

The application of Moyer et al., for "Apparatus and method for time ordering events in a system having multiple time domains" filed December 5, 2003, has been examined.

Claims 1-34 are presented for examination.

Information disclosed and listed on PTO 1449 has been considered.

Claims 1-24, 26-34 are rejected under 35 USC § 102.

Claim 25 is rejected under 35 USC § 103.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bridge et al. (U.S. Patent No. 6,125,368).

As per claim 1, Bridge discloses in a system, a method for time ordering events in the system comprising: providing control information corresponding to each of a plurality of time domains (col. 4, lines 12-16) the control information indicating when a

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timestamp message for each of the plurality of time domains is to be generated (col. 6, lines 17-23)

determining when a time domain event that requires generation of a timestamp message occurs in any one of the plurality of time domains (col. 4, lines 51-63)

generating a timestamp message corresponding to a predetermined one of the plurality of time domains in response to determining that the time domain event occurred (col. 6, lines 17-23).

As per claim 2, Bridge discloses in response to the control information, including within the timestamp message a time count in a message generating time domain that is an absolute count value of when the time domain event occurred in the message generating time domain (col. 6, lines 24-34).

As per claim 3, Bridge discloses in response to the control information, including within the timestamp message a time count in a message generating time domain that is a relative count value measured from a most recently occurring previous time domain event of when the time domain occurred in the message generating time domain (col. 6, lines 24-42).

As per claim 4, Bridge discloses in response to the control information, including within the timestamp message a time count for all of the plurality of time domains

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corresponding to when the time domain event occurred (col. 6, lines 24-42).

As per claim 5, Bridge discloses including within the timestamp message a format identifier field that identifies one of a plurality of predetermined formats that the timestamp message has (col. 6, lines 17-23).

As per claim 6, Bridge discloses using the control information to specify when a time domain event that requires generation of a timestamp message occurs in a predetermined one of the plurality of time domains (col. 4, lines 51-63)

subsequently determining when the time domain event occurs in the predetermined one of the plurality of time domains (col. 6, lines 17-23).

As per claim 7, Bridge discloses programming the control information into a storage device (col. 6, lines 7-9).

As per claim 8, Bridge discloses generating the timestamp message in response to the control information identifying predetermined operating conditions that create the time domain event in at least one of the plurality of time domains (col. 6, lines 17-23).

As per claim 9, Bridge discloses identifying the predetermined operating conditions to be at least one of a user programmable event and a programmable

system event (col. 7, lines 38-49).

As per claim 10, Bridge discloses at least one programmable system event further comprises at least one of entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value or entry into and exit from a debug mode of operation (col. 7, lines 61-67 through col. 8, lines 1-13).

Claims 11-24, 26-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Edwards (U.S. Patent No. 6,487,683).

As per claim 11, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit modules (Fig. 8) each functional circuit module (Fig. 10A, elements 200A-F) being clocked by a clock (Fig. 9, element 205) that represents a different time domain and having timestamping circuitry, the timestamping circuitry providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

an interface module coupled to each of the plurality of functional circuit modules, the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers (Fig. 10B, elements 180A-F) the predetermined event, the interface module receiving at least one timestamping message from a first time domain when the predetermined event occurs

(Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

As per claim 12, Edwards discloses the interface module further comprises: storage circuitry for storing the control information (Fig. 10B, elements 112A-F) as programmable control information that determines (col. 19, lines 22-24) the at least one operating condition that triggers the predetermined event (col. 13, lines 57-65).

As per claim 13, Edwards discloses the at least one operating condition that triggers the predetermined event further comprises at least one of: entrance into or exit from a power mode of operation, a change in source of a clock, a change in clock periodicity, a predetermined change in a hardware counter value, entry into and exit from a debug mode of operation, and occurrence of at least one user programmable event (col. 7, lines 61-67 through col. 8, lines 1-9).

As per claim 14, Edwards discloses the timestamping circuitry further comprises: a counter for determining either absolute or relative time in a corresponding functional circuit module (Fig. 6E, element 154)

time domain identification circuitry for providing a time domain identifier (Fig. 5A, elements 122, 126)

clock status circuitry for providing one or more operating characteristics of a clock in the corresponding functional circuit module (Fig. 9).

As per claim 15, Edwards discloses the timestamping circuitry further comprises circuitry for generating a code to be included in each message to identify a format of information included in a corresponding message (Fig. 6D, element 146).

As per claim 16, Edwards discloses the interface module further comprises an arbiter having circuitry for generating a code to be included in each timestamping message to identify a format of information (Fig. 6D, element 146) included in a corresponding timestamping message (Fig. 6D, element 148).

As per claim 17, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a time count value (Fig. 6E, element 154) that is an absolute value referenced to a known starting value, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the timestamping message (Fig. 6D, element 148).

As per claim 18, Edwards discloses the message has a format that further comprises a field that identifies that the format of the timestamping message has an

absolute value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 19, Edwards discloses the message provided by at least one of the plurality of functional circuit modules (Fig. 10A) has a format that comprises at least a time count value (Fig. 6E, element 154) that is a relative value referenced to a last occurring predetermined event, status information of a clock signal associated with one of the functional circuit modules (col. 19, lines 38-46) and an identifier that indicates a corresponding time domain associated with the timestamping message (Fig. 6D, element 148).

As per claim 20, Edwards discloses the message has a format that further comprises a field that identifies that the format of the timestamping message having a relative value time count value (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 21, Edwards discloses the timestamping message has a format that comprises a time count value corresponding to each of the functional circuit modules and predetermined status information associated with each of the functional circuit modules when the predetermined event occurs (Fig. 6D, element 146, 148) and (Fig. 6E, element 154).

As per claim 22, Edwards discloses the control information is programmable (col. 19, lines 22-24).

As per claim 23, Edwards discloses the interface module further comprises: at least one register for storing the control information (Fig. 10B, elements 112A-F).

As per claim 24, Edwards discloses the interface module provides timestamping messages from all time domains at a common interface port (Fig. 10A).

As per claim 26, Edwards discloses a system for time ordering events comprising: a plurality of functional circuit module (Fig. 8) means, each being clocked by a clock that represents a different time domain and having timestamping circuit means (Fig. 10A, elements 200A-F), the timestamping circuit means providing a message that indicates a point in time when a predetermined event occurs (Fig. 6D, element 148)

interface module means coupled to each of the plurality of functional circuit module means (Fig. 10B, elements 180A-F) the interface module means providing control information to the plurality of functional circuit module means to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module means receiving at least one timestamping message from a first time domain when the predetermined event occurs (Fig. 10B, elements 112A-F) in one of a plurality of time domains including the first time domain (Fig. 6D, element 148).

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As per claim 27, Edwards discloses the timestamping messages from all time domains are provided by interface module means at a common interface port means (Fig. 10A).

As per claim 28, Edwards discloses a system comprising: a plurality of functional circuit modules (Fig. 8 and 10A-B) on a same integrated circuit (col. 4, lines 16-18), each functional circuit module being clocked by a clock (Fig. 9, element 205) that represents a different time domain, and each functional module having timestamping circuitry operating at independent clock rates for providing timestamp messages (Fig. 6D, element 148).

As per claim 29, Edwards discloses the timestamp messages each indicate a point in time when a predetermined event occurs (Fig. 6D, element 148).

As per claim 30, Edwards discloses an interface module coupled to each of the plurality of functional circuit modules (Fig. 10B, elements 180A-F) the interface module providing control information to the plurality of functional circuit modules to indicate at least one operating condition that triggers the predetermined event (Fig. 10B, elements 180A-F) the interface module receiving at least one timestamping message (Fig. 6D, element 148) from a first time domain when the predetermined event occurs in one of a plurality of time domains including the first time domain (Fig. 6E, element 156).

As per claim 31, Edwards discloses a method of reconstructing time ordering of events that occur in multiple time domains in a system, the method comprising: receiving multiple timestamping messages (Fig. 6D, element 148) in one of an ordered time sequence and an unordered time sequence; tracking relative count values of multiple time domain counters (Fig. 5B, element 126) and (Fig. 6E, element 156) and (Fig. 6F, element 158) associated with the multiple time domains and operating at independent clock rates; and sorting debug information in time ordered sequence, the debug information being associated with a timestamp (Fig. 6D, element 148) provided from one of the multiple time domains (Fig. 3, elements 72, 32).

As per claim 32, Edwards discloses providing the debug information via a debug message (Fig. 3, elements 72, 32).

As per claim 33, Edwards discloses implementing the debug messages as at least one of a program trace message, a data trace message and a watchpoint message (Fig. 3) and (col. 14, lines 34-52).

As per claim 34, Edwards discloses generating the multiple timestamp messages (Fig. 6D, element 148) by: providing control information corresponding to each of multiple time domains (Fig. 6C, 6D), the control information indicating when a timestamp message for each of the multiple time domains is to be generated (Fig. 6D, element 148) determining when a time domain event that requires generation of a

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timestamp message occurs in any one of the multiple time domains (Fig. 6E, element 154) and generating a timestamp message corresponding to a predetermined one of the multiple time domains in response to determining that the time domain event occurred (Fig. 6D, element 148).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (U.S. Patent No. 6,487,683) in view of Rohfleisch et al. (U.S. Patent No. 7,058,855).

As per claim 25, Edwards fails to explicitly disclose IEEE ISTO 5001 (NEXUS).

Rohfleisch teaches:

the common interface port of the interface module meets IEEE ISTO 5001 (NEXUS) compliance (col. 7, lines 65-67 through col. 8, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of System-on-chip debugging of Edwards in combination with the on-chip debugging system of Rohfleisch et al. to provide debugging information.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Edwards discloses a debugging system for System-on-chip devices (Fig. 1). Rohfleisch et al. teaches of the on-chip debugging system of integrated circuit (Fig. 1) and (col. 7, lines 60-65). Edwards uses the method of generating timestamp messages to identify events (Fig. 6D, element 148). Rohfleisch et al. also discloses a method of using timestamps (col. 8, lines 9-22).

### **Related Prior Art**

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Chen et al. (U.S. Patent No. 5,642,478), "Distributed trace data acquisition system".

Liu et al. (U.S. Patent No. 6,282,673), "Method of recording information system events".

Easterday (U.S. Patent No. 4,731,768), "Autoranging time stamp circuit".

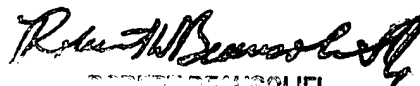
Goldring (U.S. Patent No. 5,613,113), "Consistent recreation of events from activity logs".

### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
ROBERT W. BEAUSOLIEL  
SENIOR PATENT EXAMINER  
EBC/CENTER 2100